# SYSTEM AND METHOD OF MAINTAINING HIGH BANDWIDTH REQUIREMENT OF A DATA PIPE FROM LOW BANDWIDTH MEMORIES

## ABSTRACT

A Network Processor includes a Fat Pipe Port and a memory sub-system that provides sufficient data to satisfy the Bandwidth requirements of the Fat Pipe Port. The memory sub-system includes a plurality of DDR DRAMs controlled so that data is extracted from one DDR DRAM or simultaneously from a plurality of the DDR DRAMs. By controlling the DDR DRAMs so that the outputs provide data serially or in parallel, the data Bandwidth is adjustable over a wide range. Similarly, data is written serially into one DDR DRAM or simultaneously into multiple DDR DRAMs. As a consequence buffers with data from the same frame are written into or read from different DDR DRAMs.